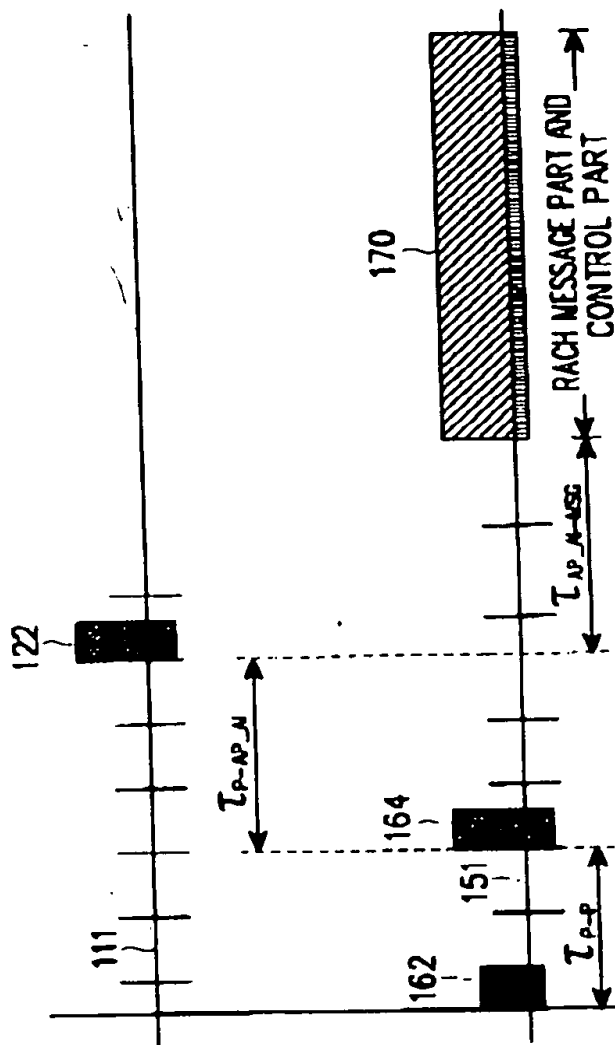


FIG. 1



The diagram illustrates the timing of a TDMA frame structure. It shows a sequence of time slots on a timeline, with various durations labeled as T_{p1} , T_{p2} , T_{p3} , T_{p4} , T_{p5} , and T_{p6} . The slots are labeled with numbers 201 through 221. The slots are divided into three main sections: a preamble section (201-206), a power control and pilot section (207-209), and a message and control part section (210-221). The preamble section includes a preamble (201) and a power control preamble (202-206). The power control and pilot section includes a power control and pilot (207-209). The message and control part section includes a message and control part (210-221). The durations T_{p1} through T_{p6} represent the time intervals between the start of the slots. The durations T_{p1} through T_{p6} are labeled as follows: T_{p1} (201), T_{p2} (202), T_{p3} (203), T_{p4} (204), T_{p5} (205), and T_{p6} (206). The durations T_{p1} through T_{p6} are labeled as follows: T_{p1} (201), T_{p2} (202), T_{p3} (203), T_{p4} (204), T_{p5} (205), and T_{p6} (206).

FIG. 4A

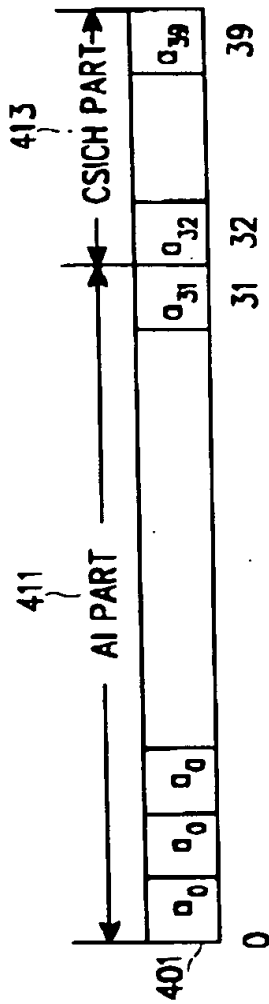
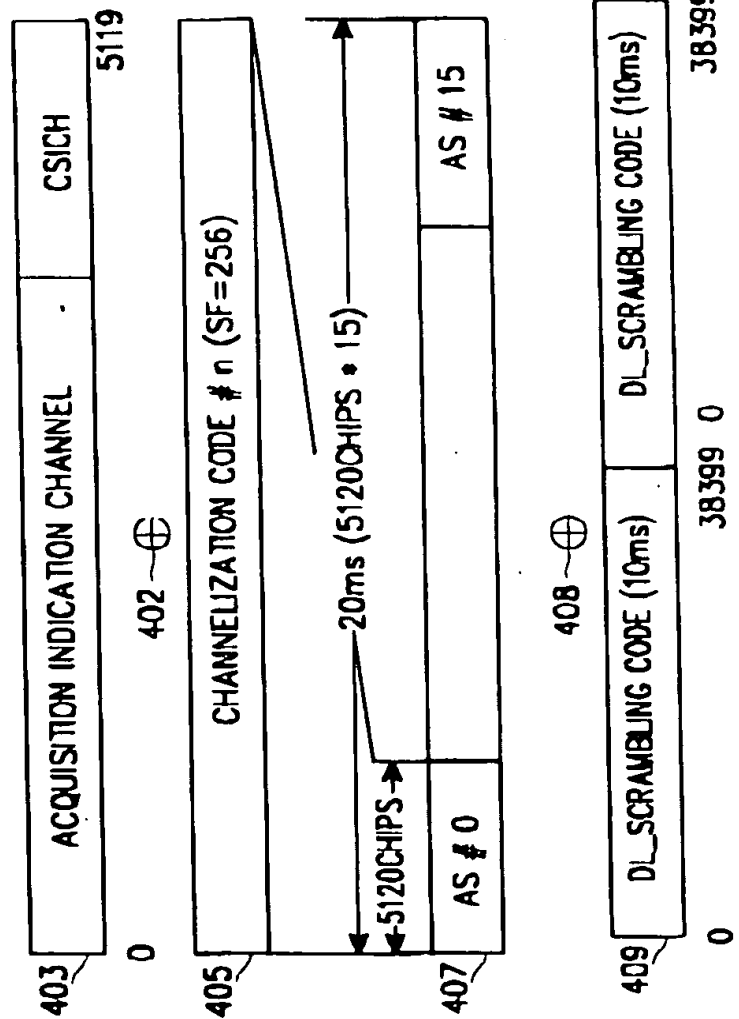


FIG. 4B



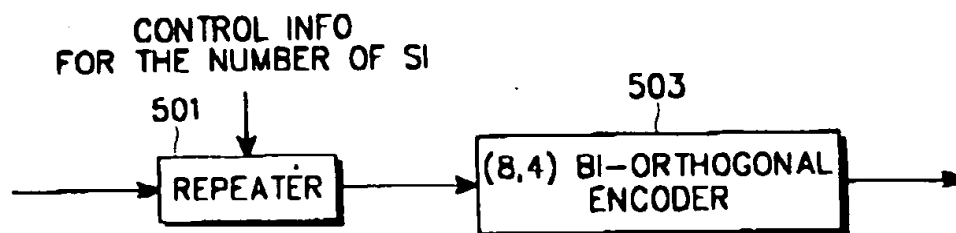


FIG. 5

09514590.070700

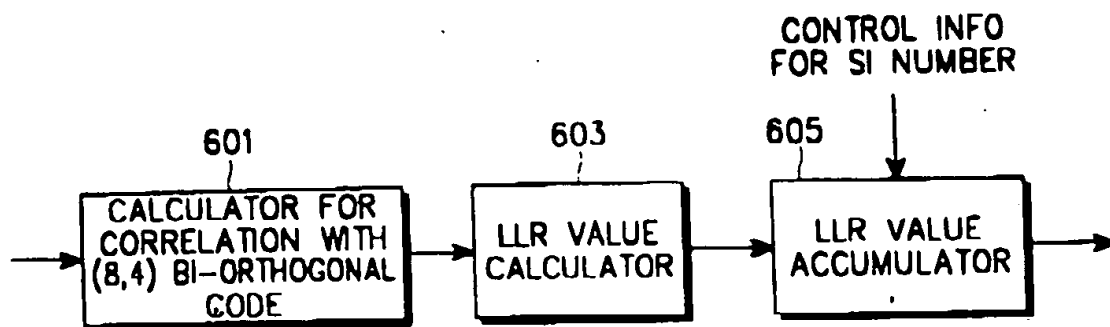


FIG. 6

09644590-070700

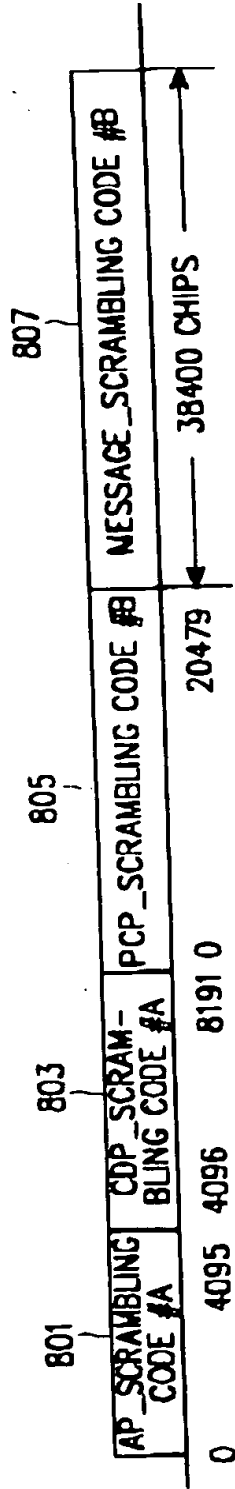


FIG. 8A

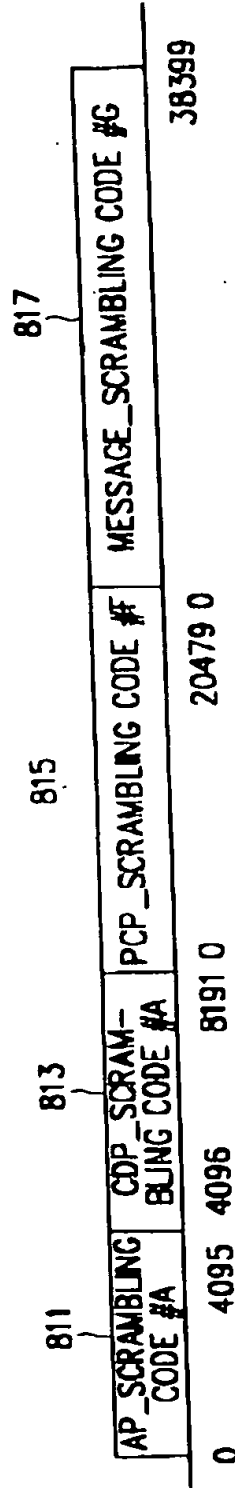


FIG. 8B

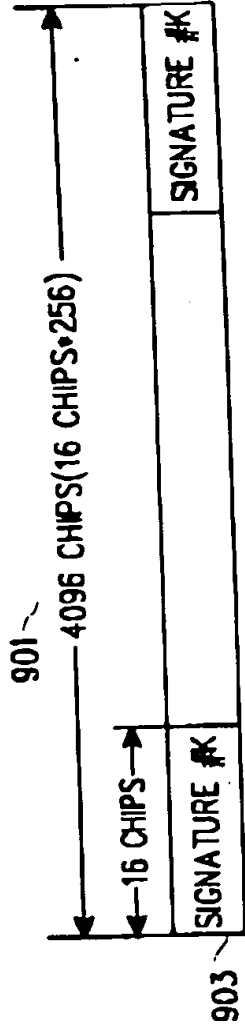


FIG. 9A

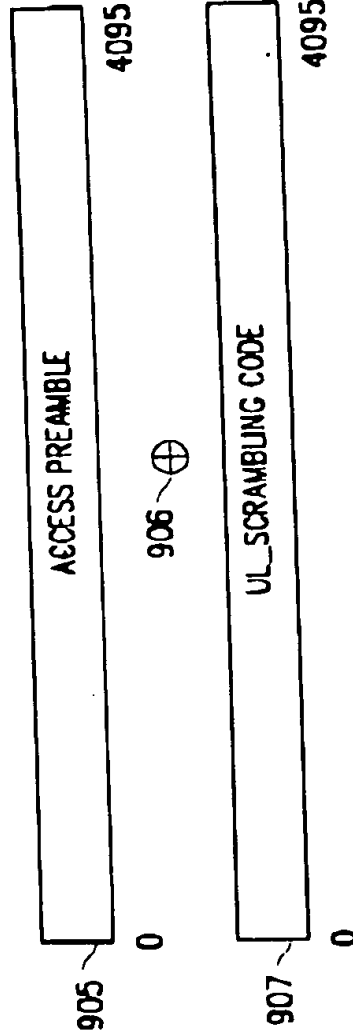


FIG. 9B

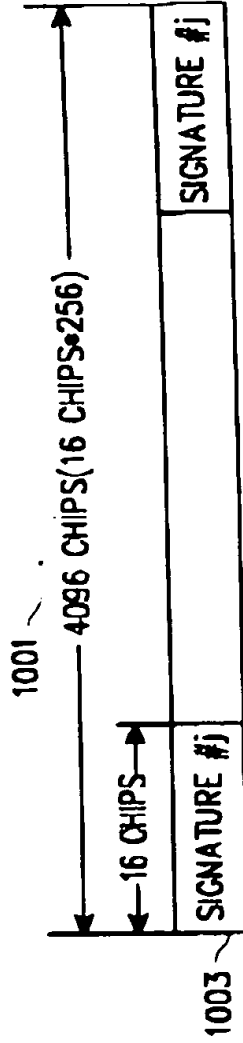


FIG. 10A

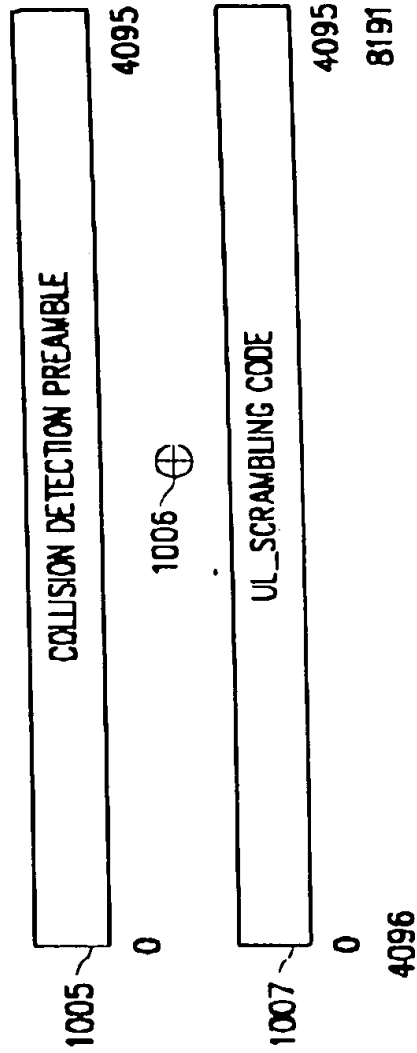


FIG. 10B

FIG. 11A

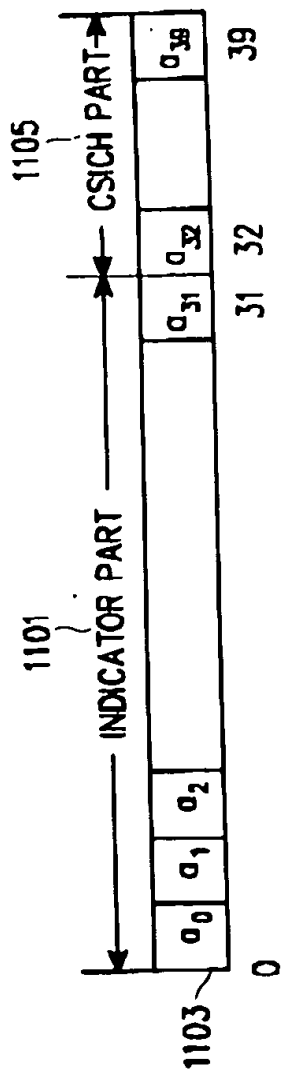
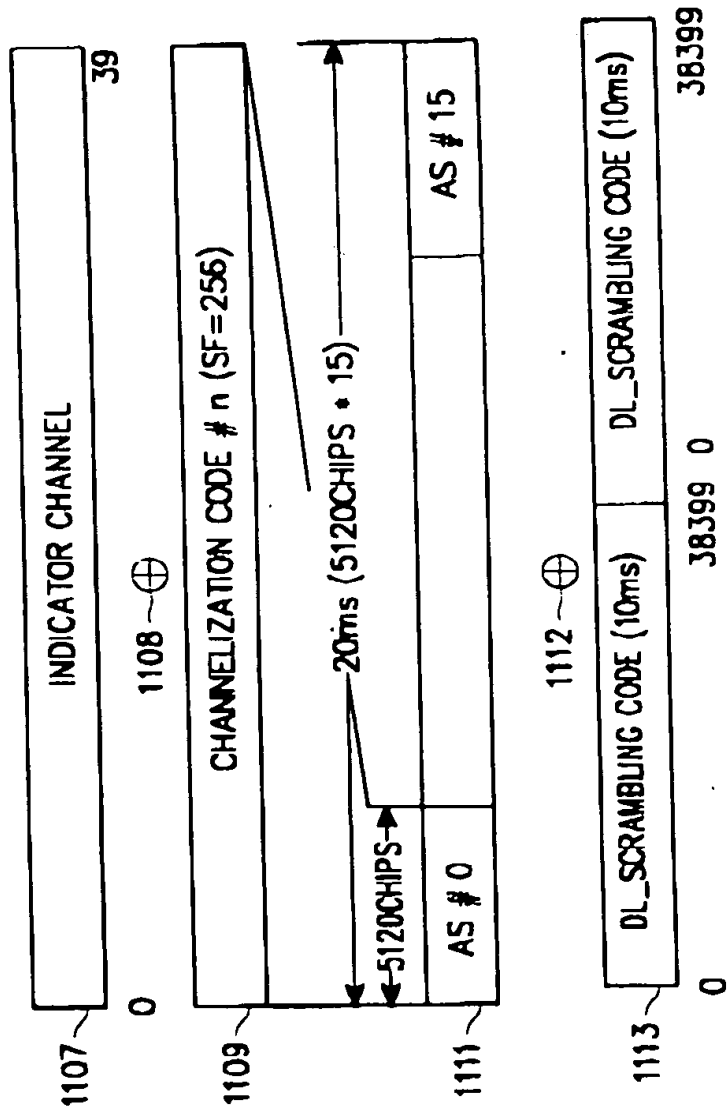


FIG. 11B



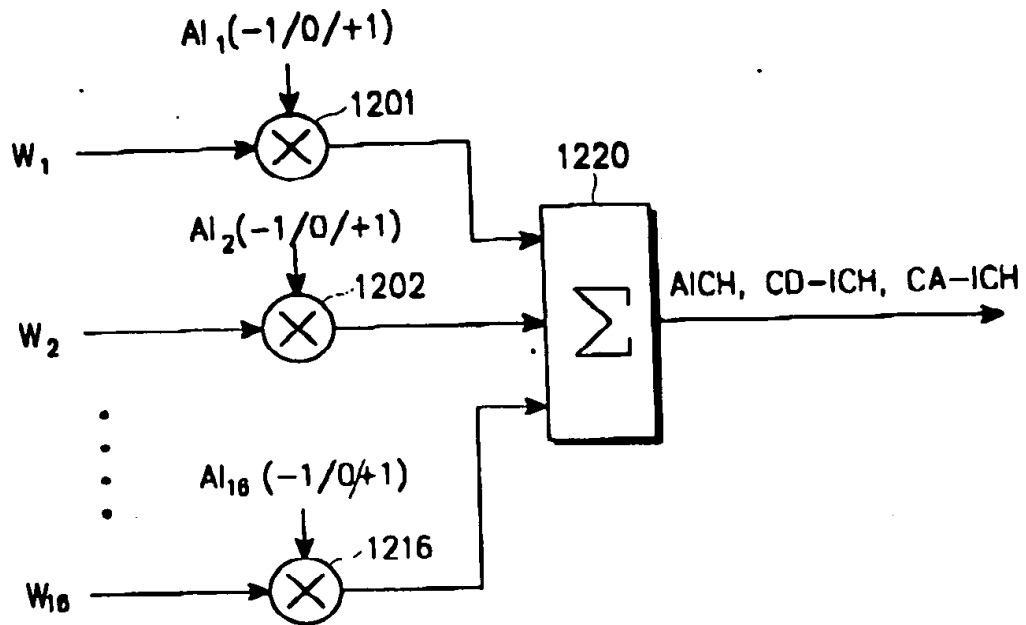


FIG. 12

FIG. 13A

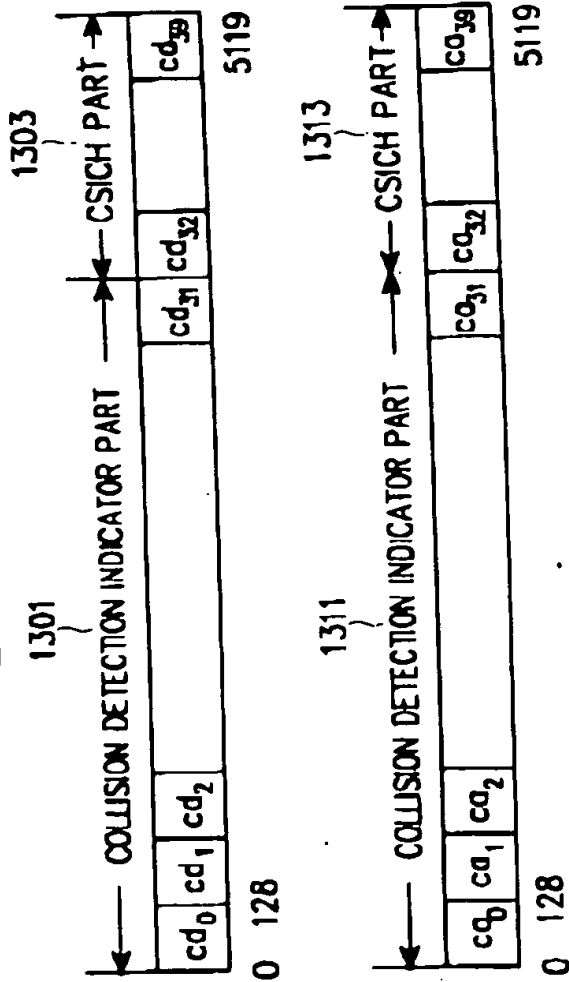
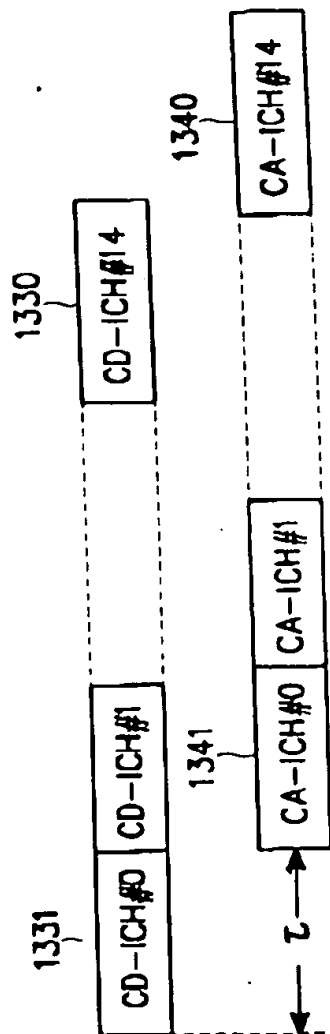


FIG. 13B



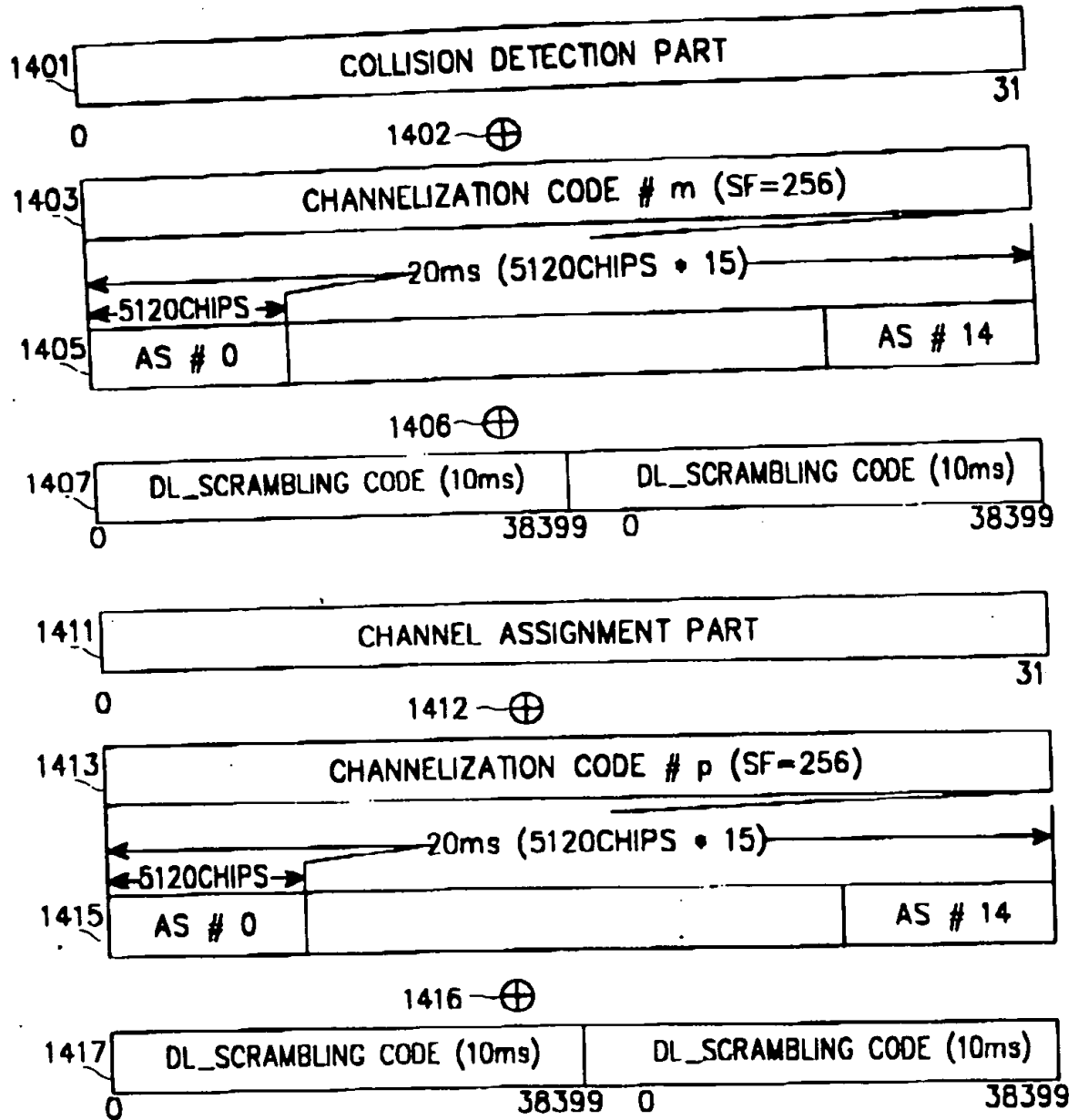


FIG. 14

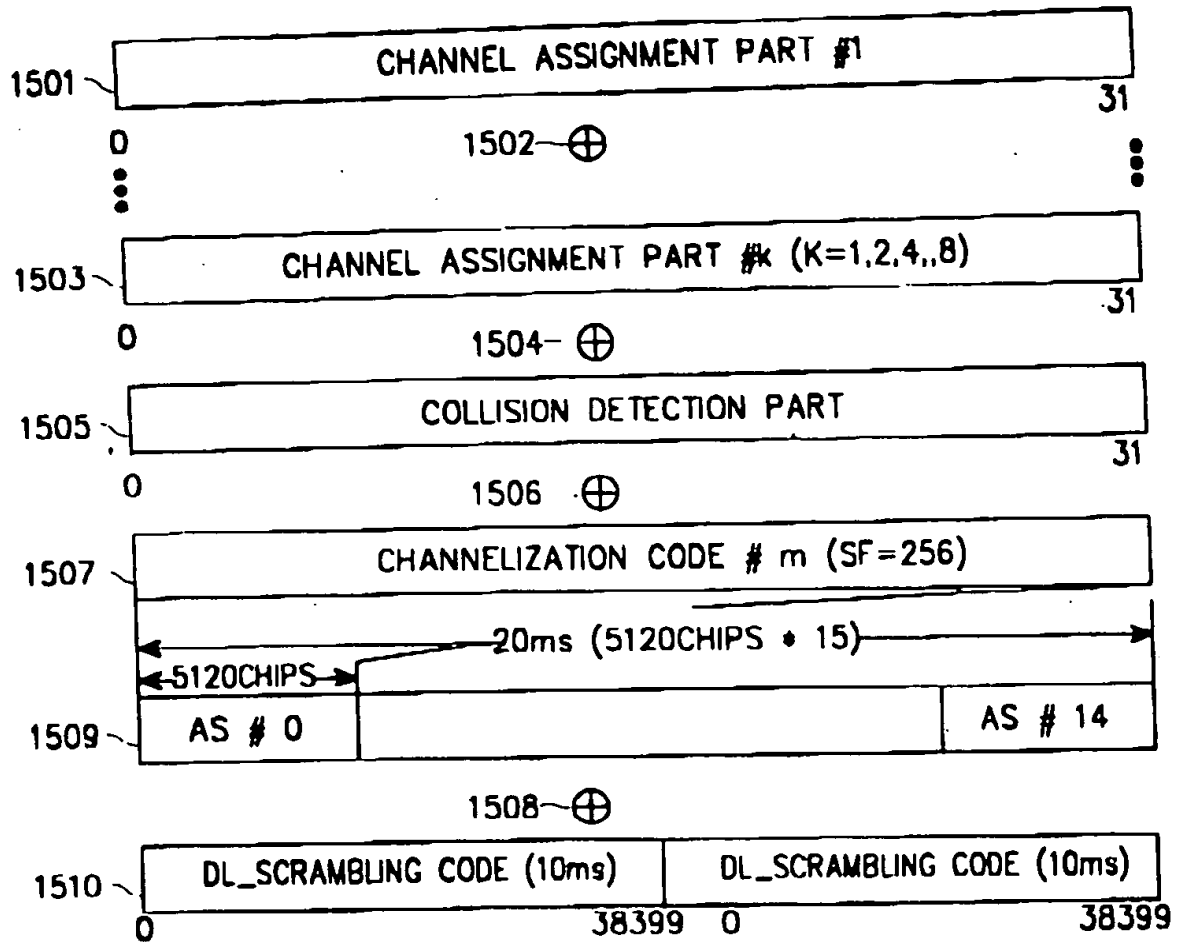
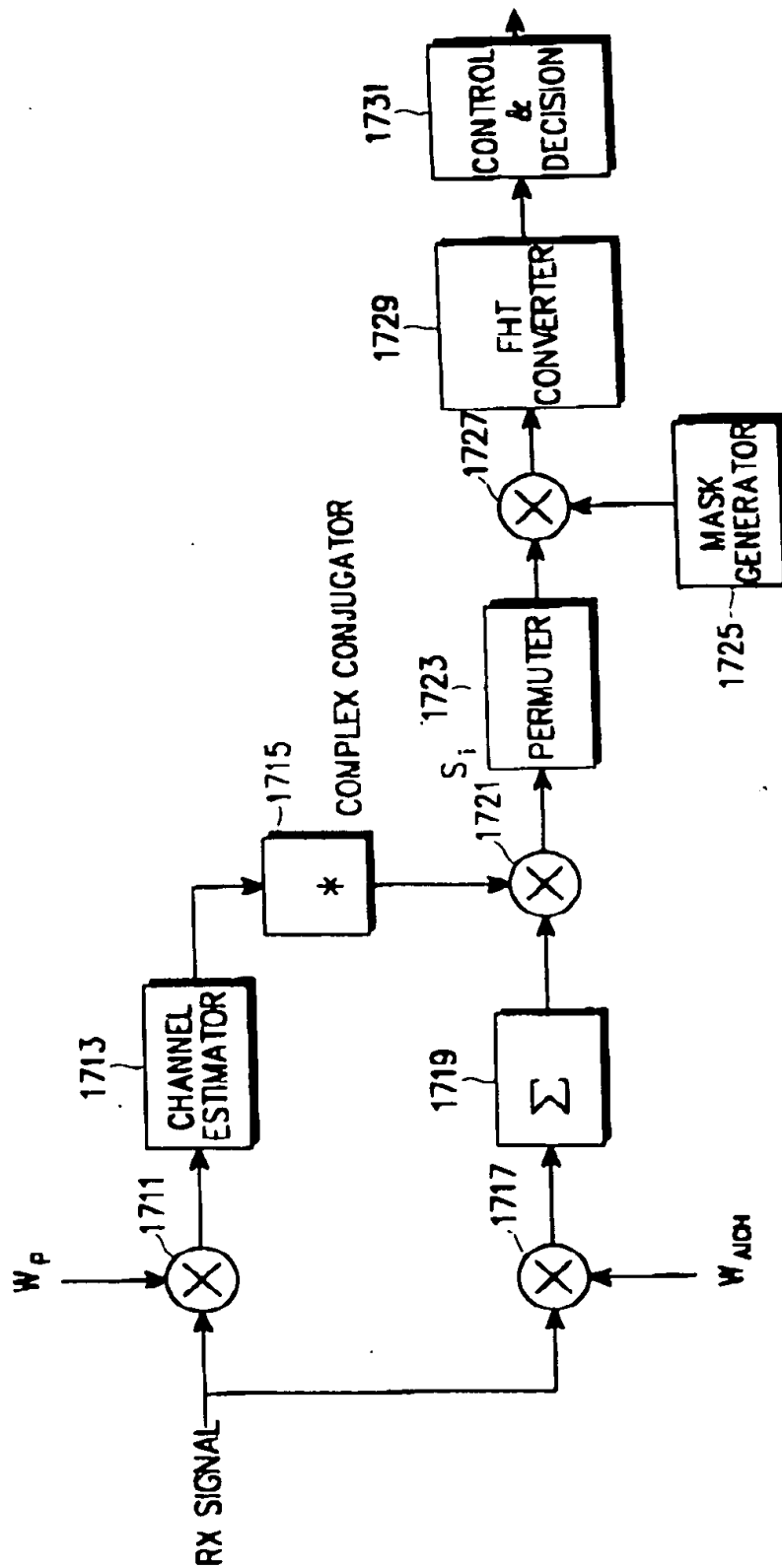


FIG. 15

FIG. 17



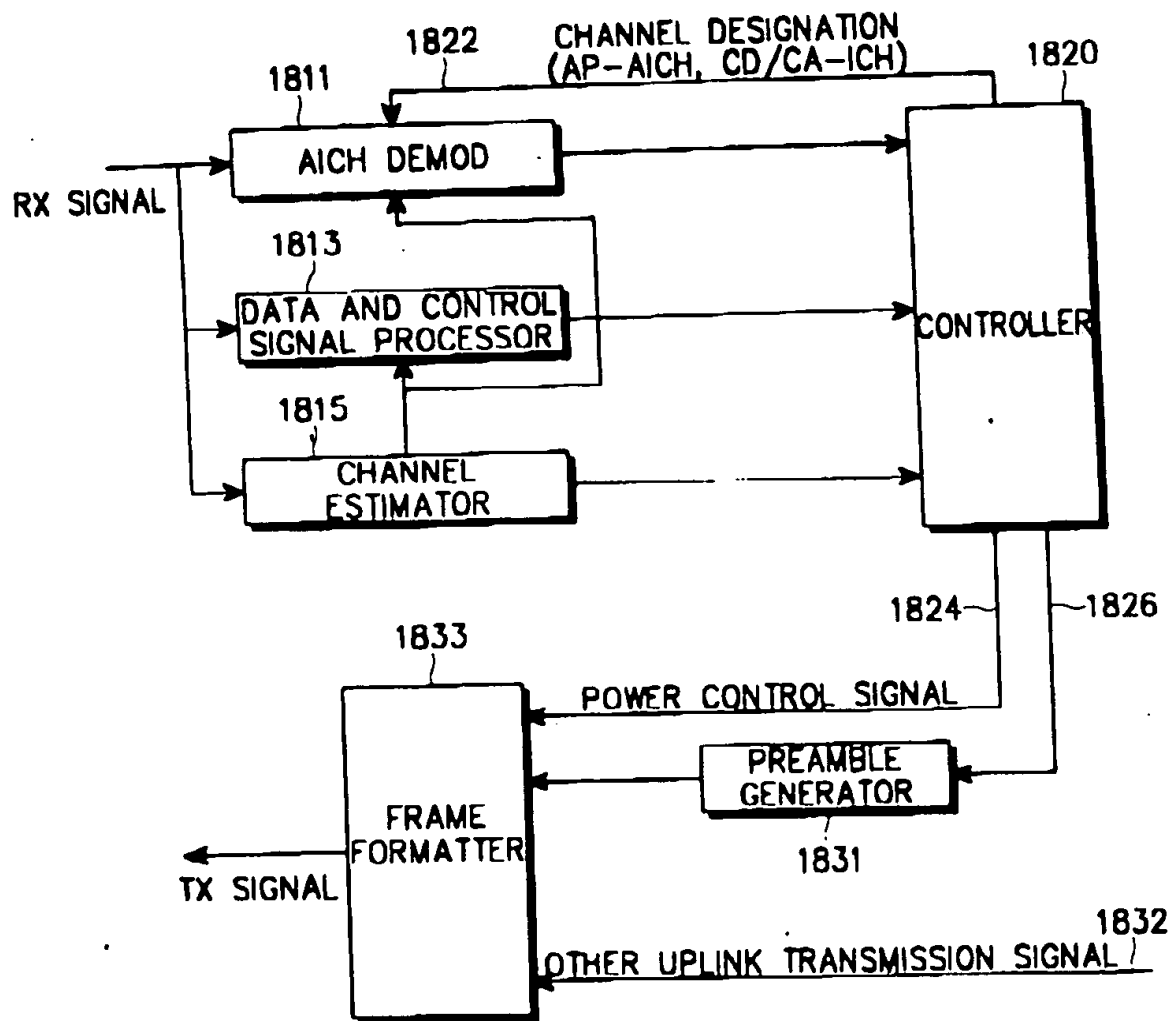


FIG. 18

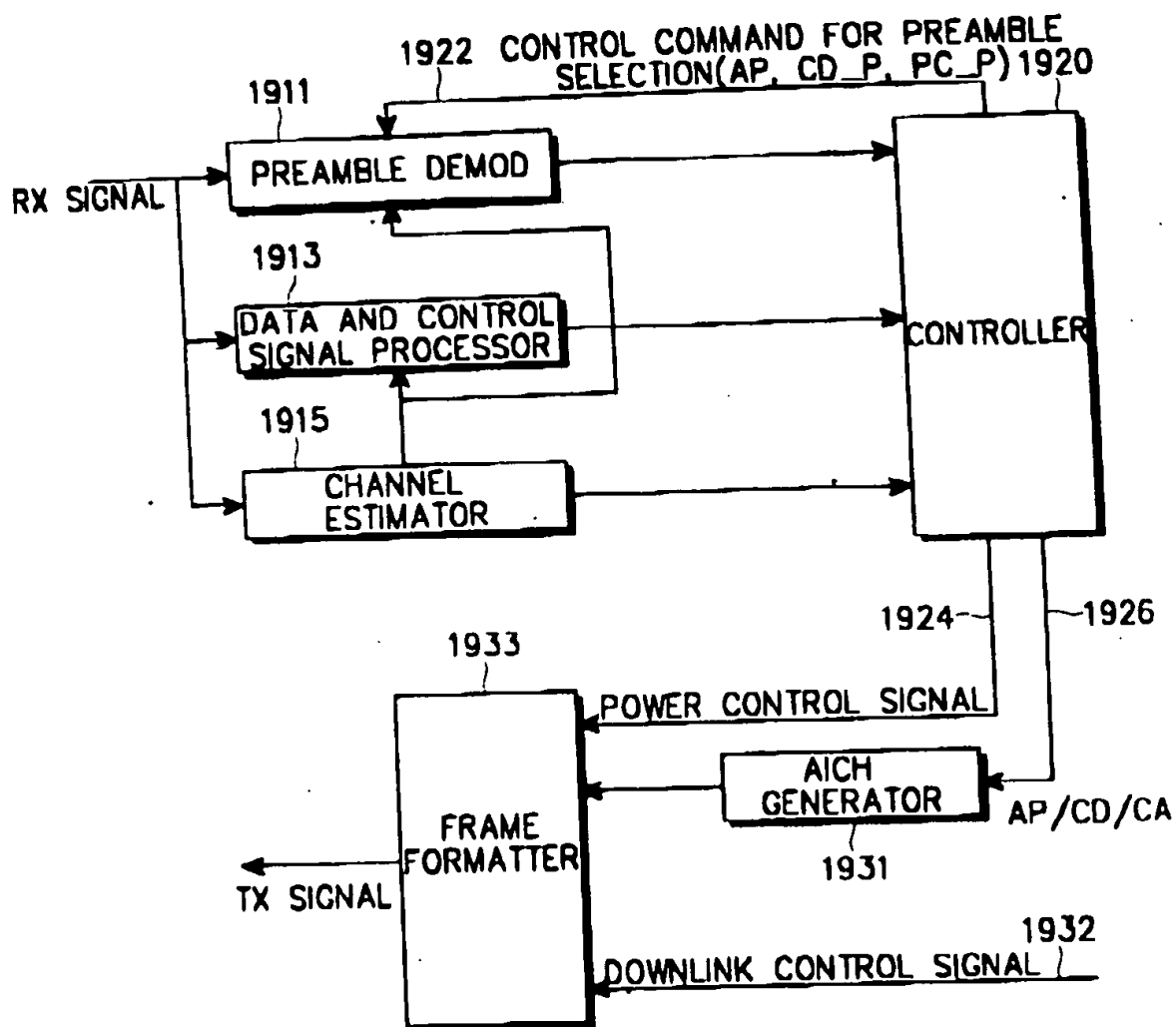
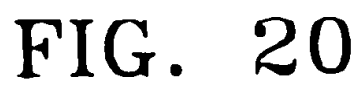


FIG. 19



004040" 05M1F360

FIG. 21

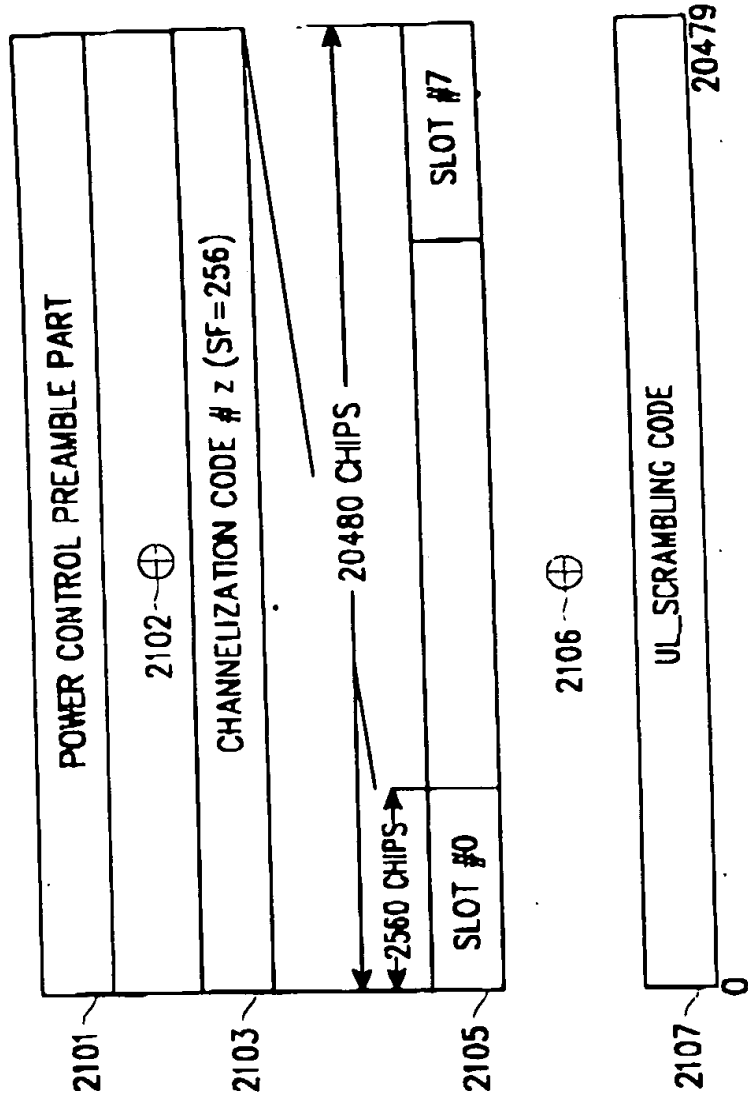


FIG. 22B

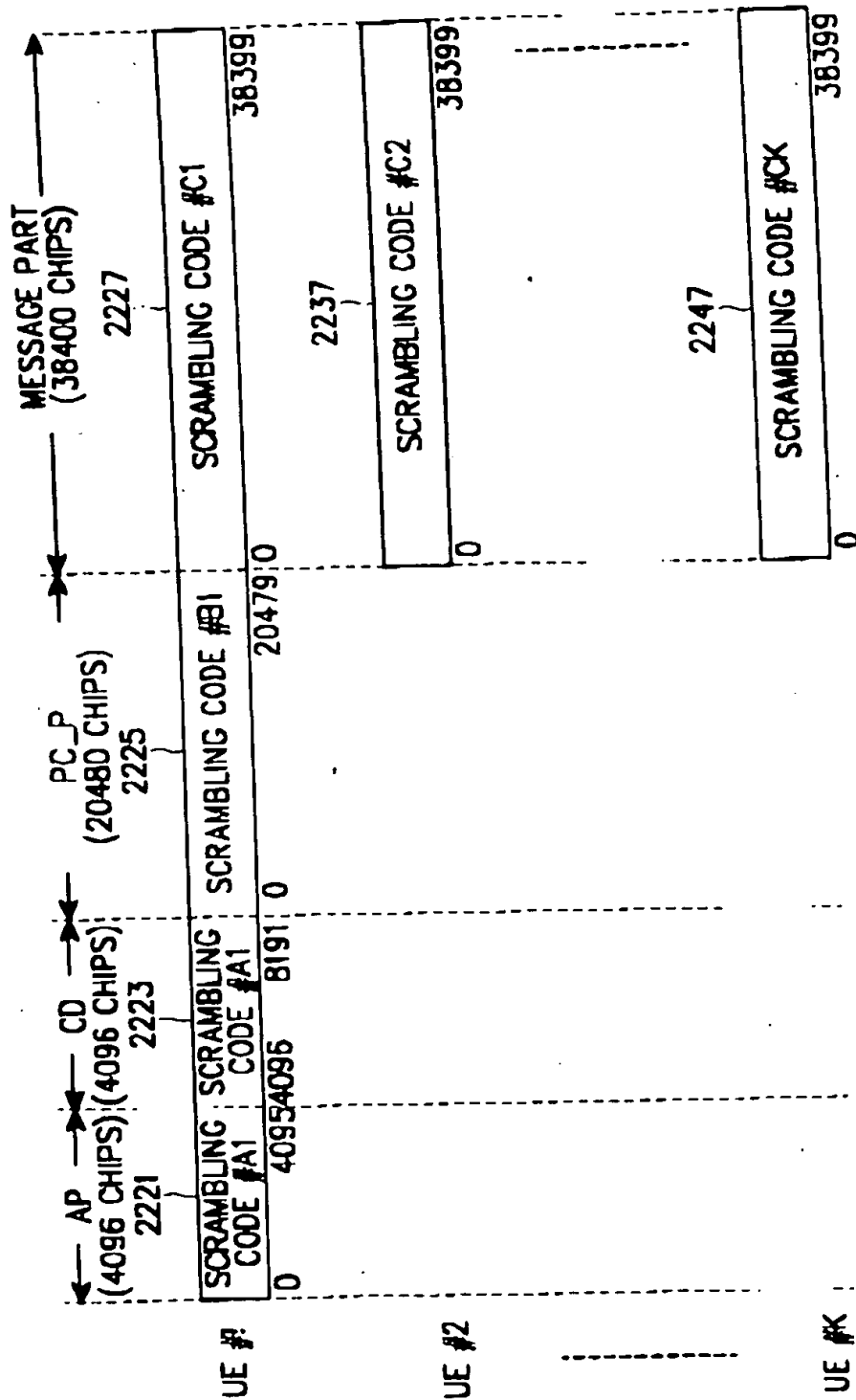


FIG. 23

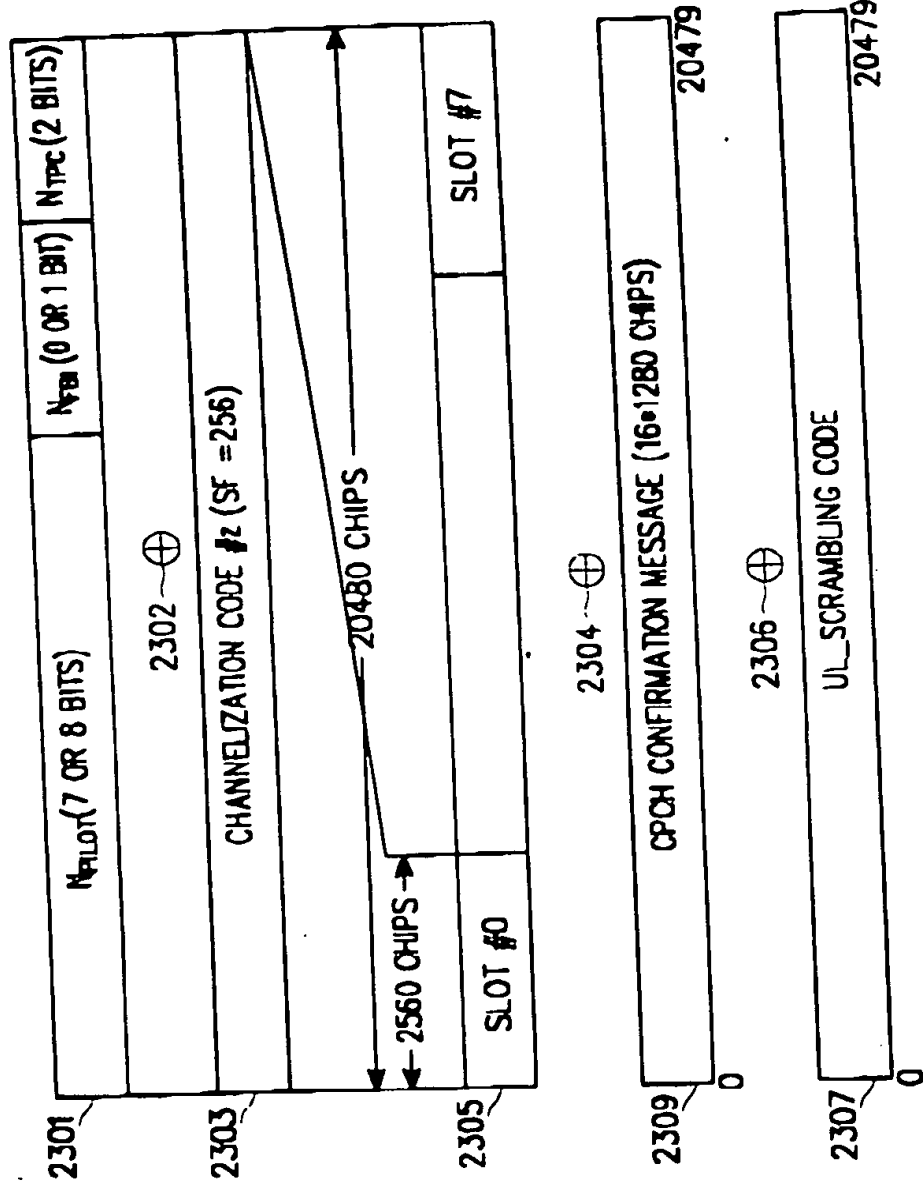


FIG. 24A

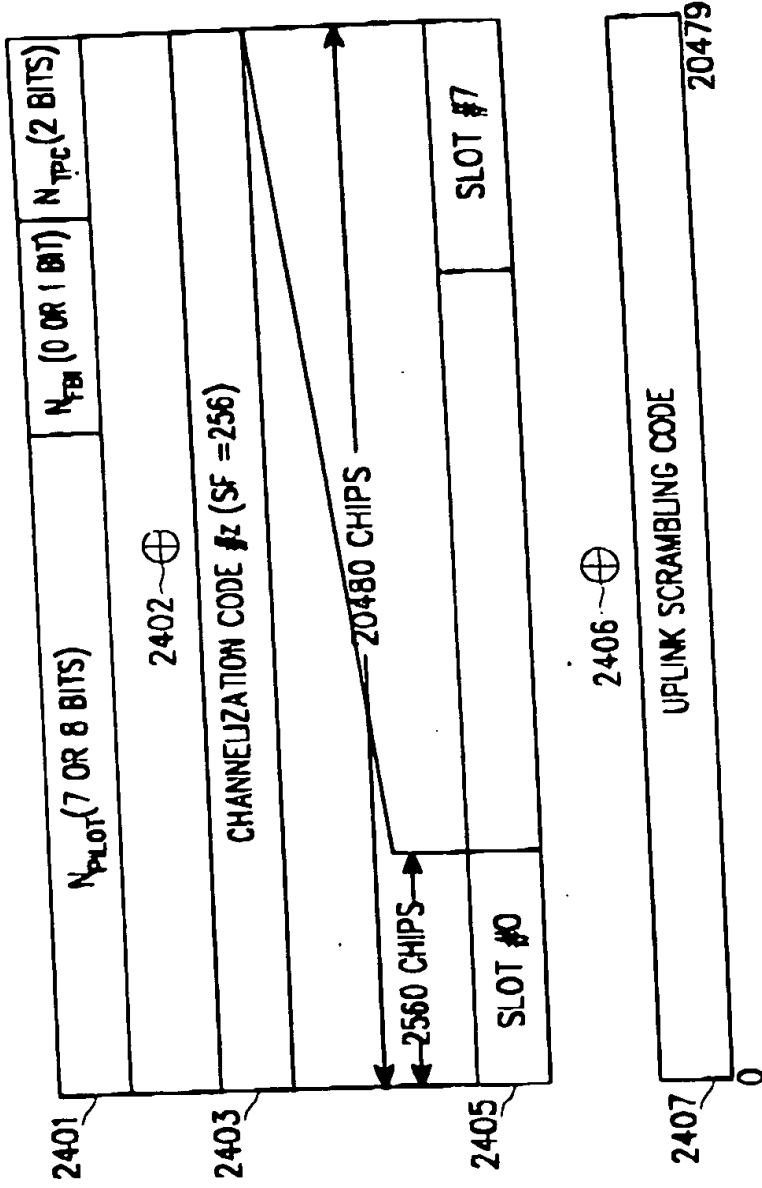


FIG. 24B

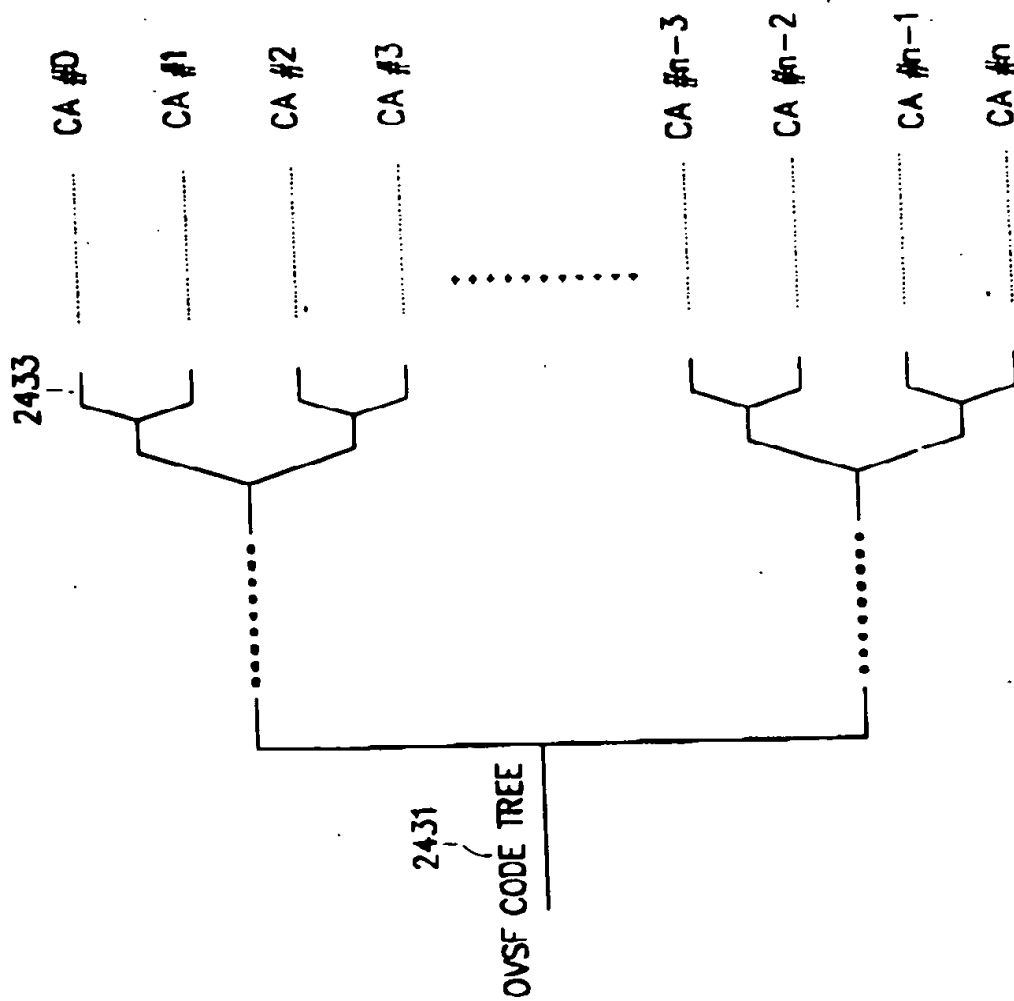


FIG. 25A

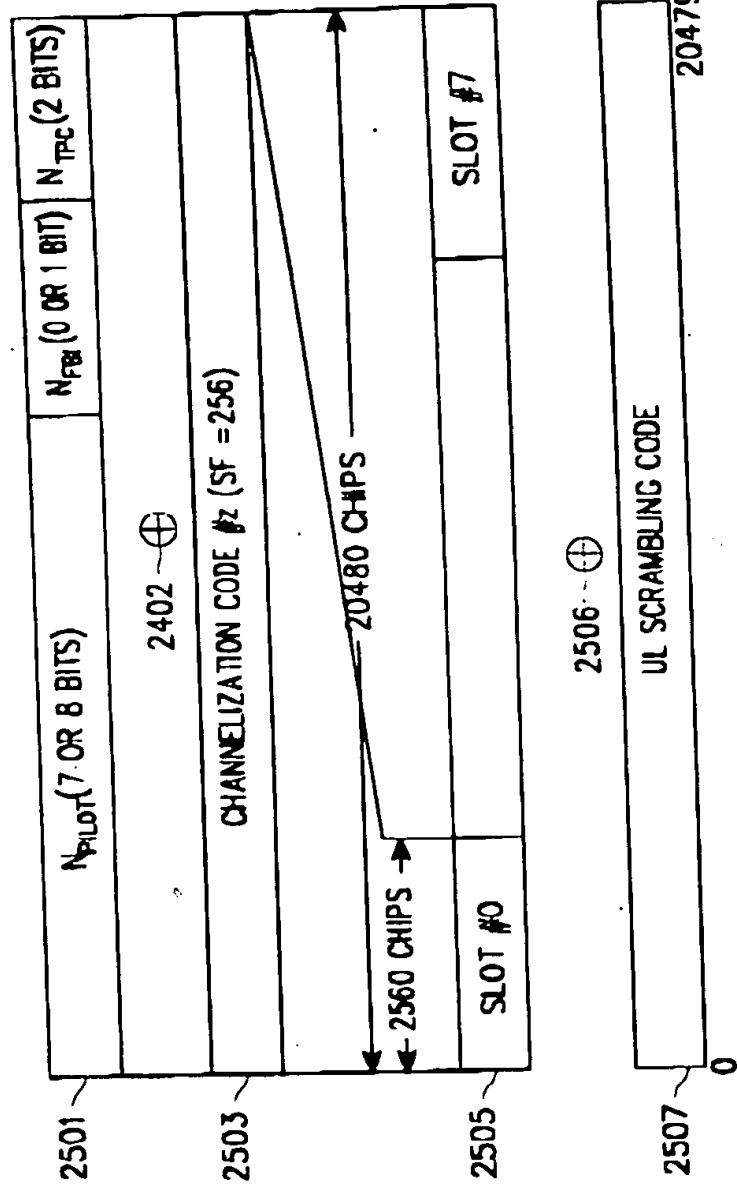


FIG. 25B

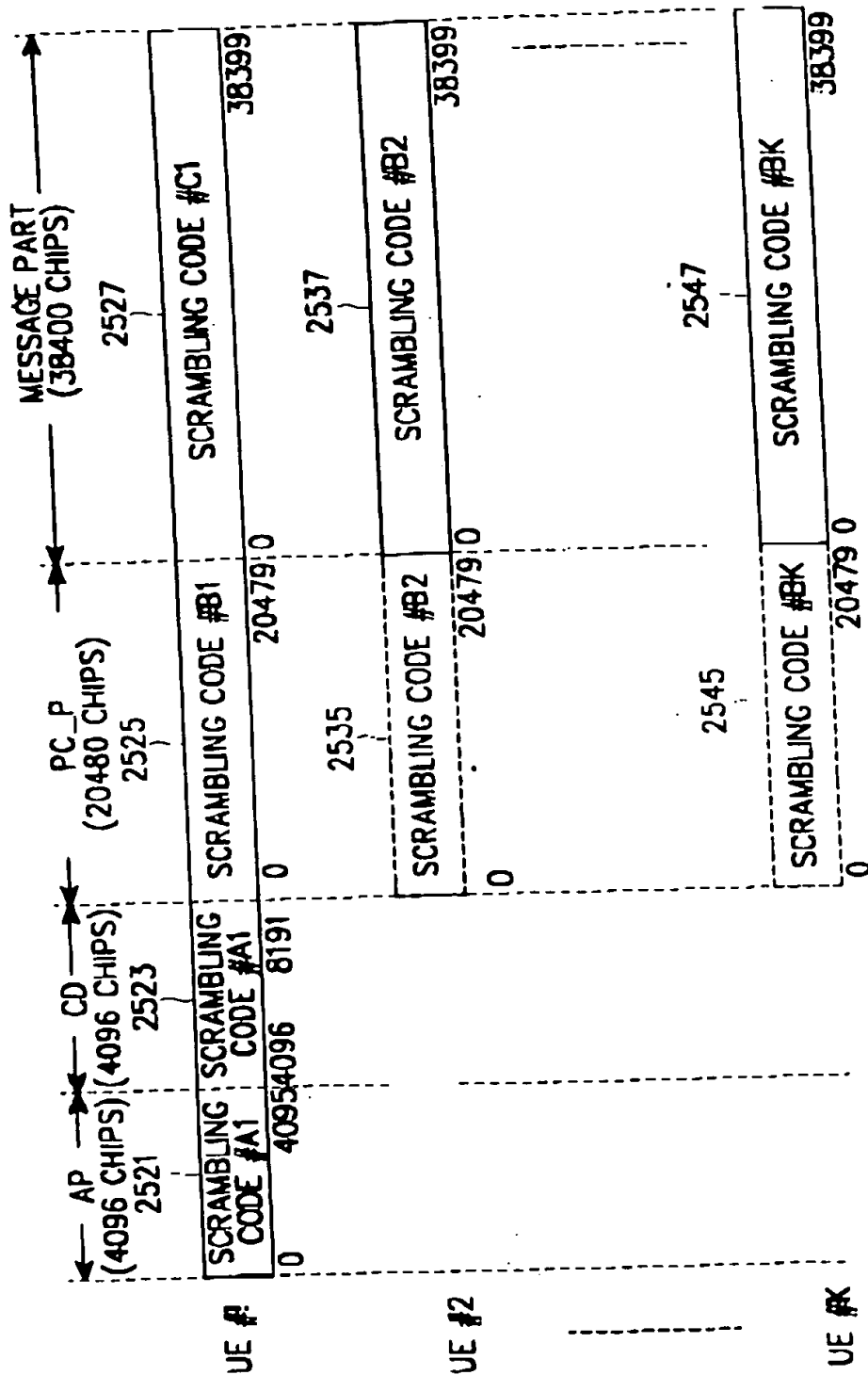
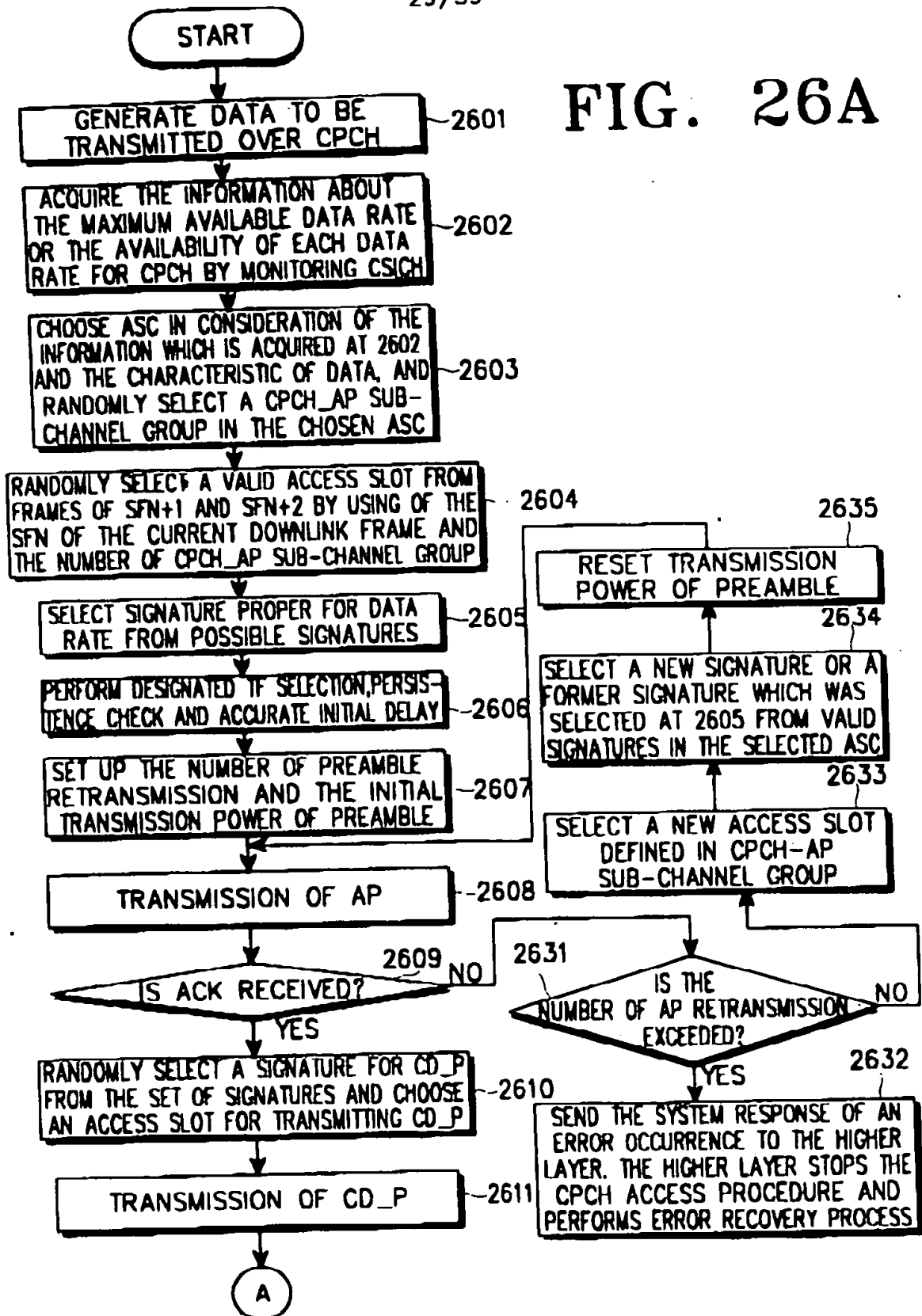


FIG. 26A



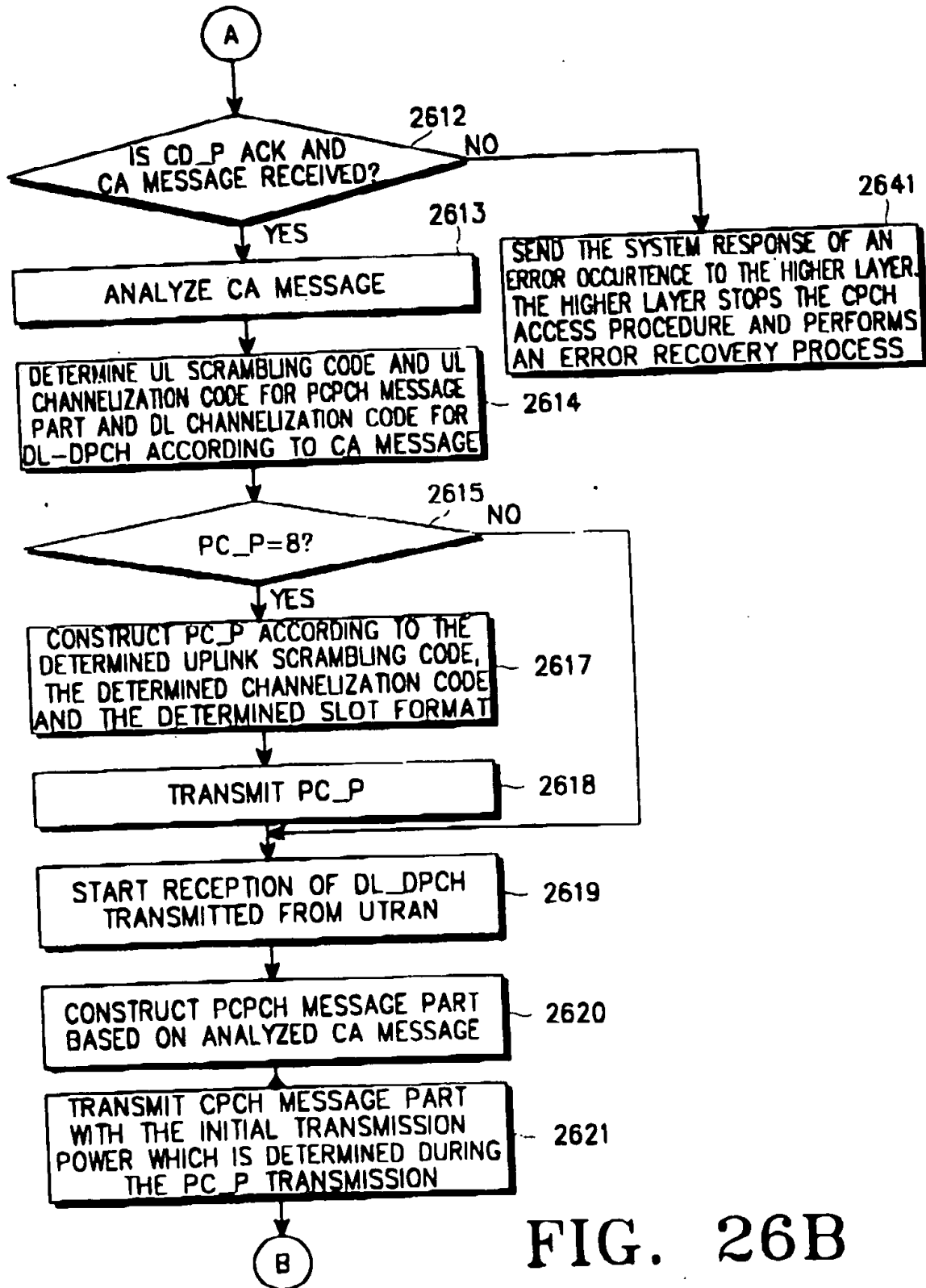


FIG. 26B

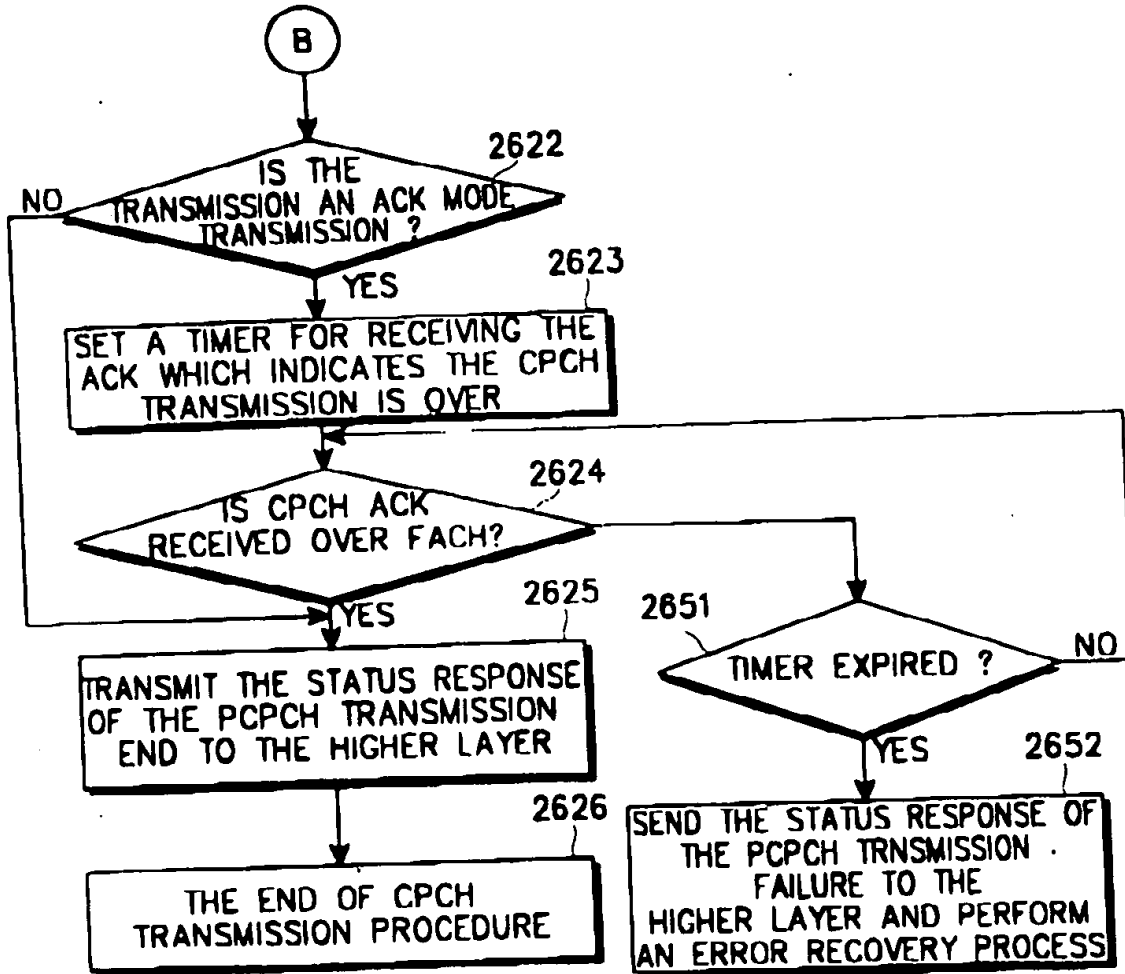
FLOWCHART OF CPCH USING CHANNEL ASSIGNMENT
(UTRAN SIDE)

FIG. 26C

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FLOWCHART OF CPCH USING CHANNEL ASSIGNMENT
(UTRAN SIDE)

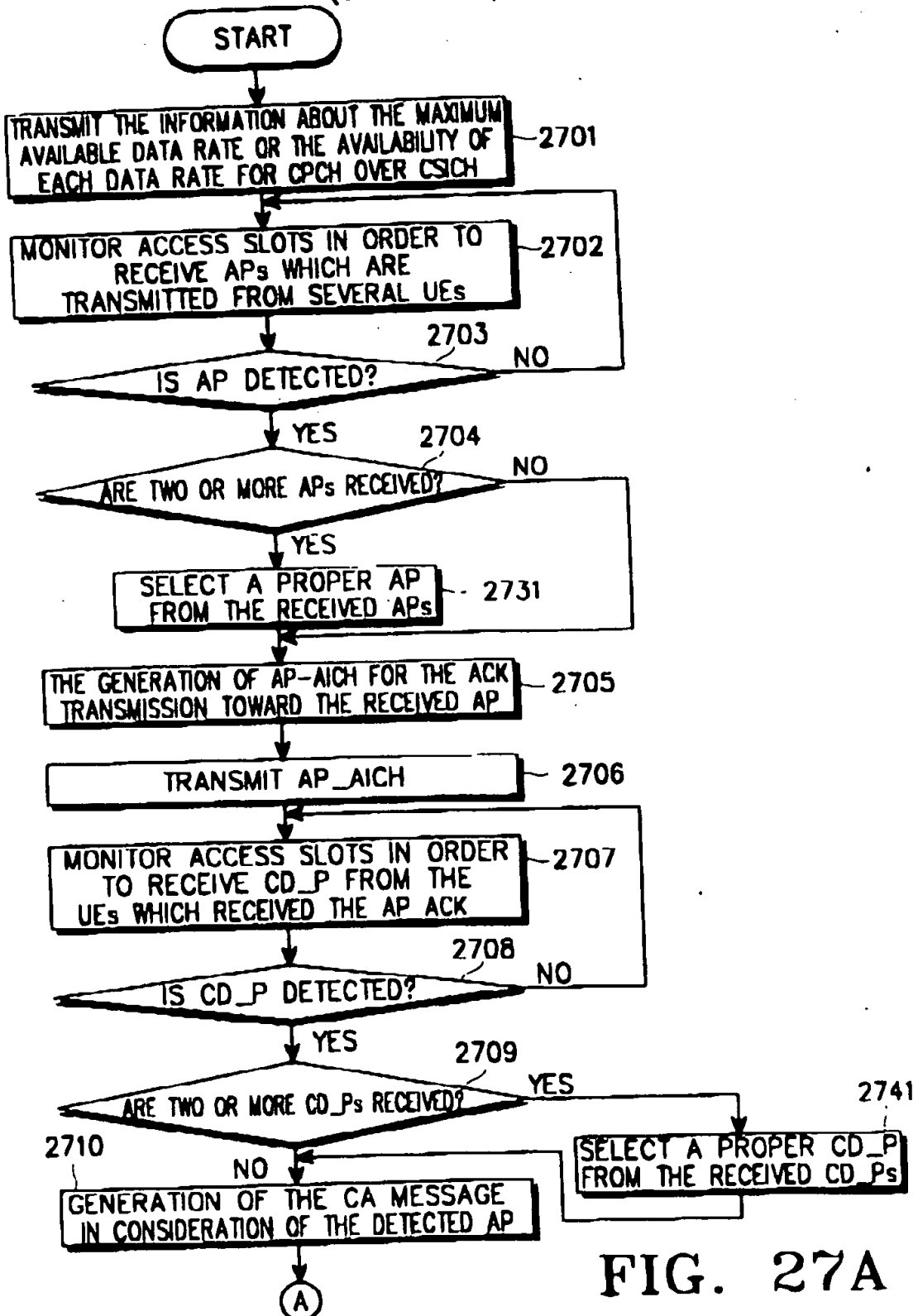


FIG. 27A


```

graph TD
    A((A)) --> 2711[GENERATION OF THE CD/CA_I CH FOR TRANSMITTING THE CA MESSAGE AND THE ACK FOR THE DETECTED CD_P]
    2711 --> 2712[TRANSMIT CD/CA_I CH]
    2712 --> 2713[GENERATION OF DL_DPCH IN ORDER TO CONTROL THE CD_P TRANSMISSION POWER]
    2713 --> 2714[TRANSMIT DL_DPCH]
    2714 --> 2715{PC_P LENGTH = 0?}
    2715 -- YES --> 2719[START THE RECEPTION OF PCPCH MESSAGE PART]
    2715 -- NO --> 2716[GENERATE THE POWER CONTROL COMMAND IN ORDER TO CONTROL THE PC_P BY TAKING INTO ACCOUNT THE TRANSMISSION POWER OF RECEIVED PC_P]
    2716 --> 2717[TRANSMIT GENERATED POWER CONTROL COMMAND OVER DL_DPCCH]
    2717 --> 2718{IS THE RECEPTION OF PC_P OVER?}
    2718 -- NO --> 2716
    2718 -- YES --> 2719
    2719 --> 2720{IS THE RECEPTION OF THE PCPCH MESSAGE PART OVER?}
    2720 -- NO --> 2719
    2720 -- YES --> B((B))
  
```

FIG. 27B

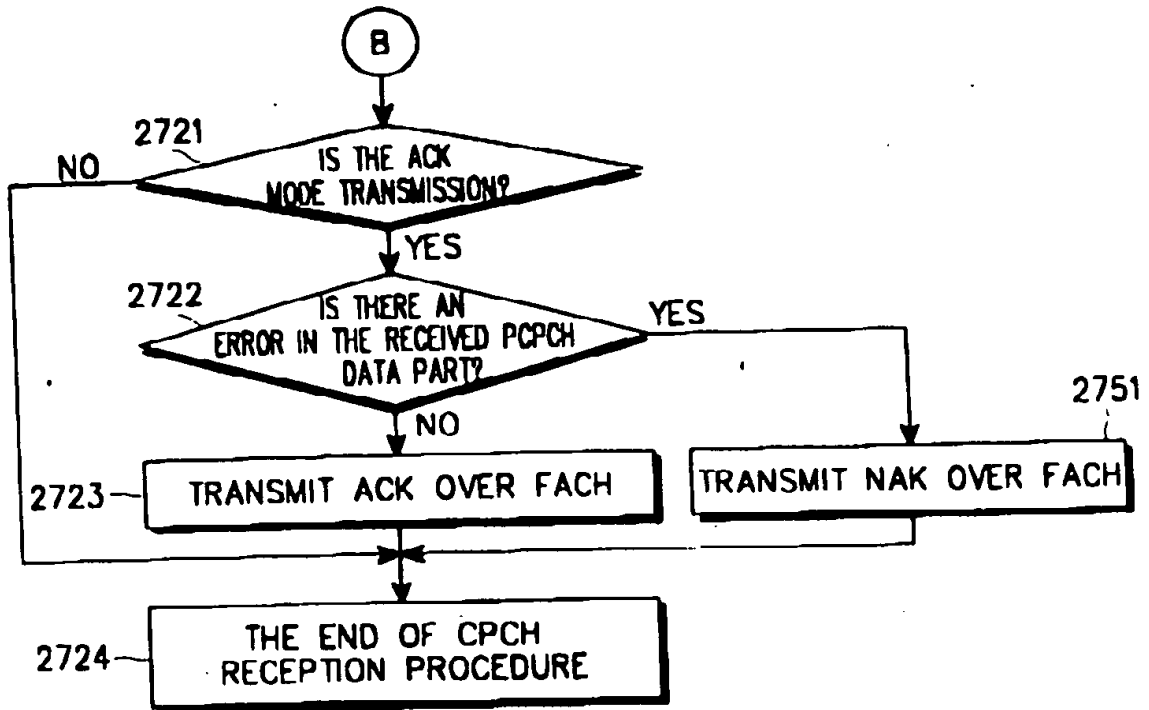
FLOWCHART OF CPCH USING CHANNEL ASSIGNMENT
(UTRAN SIDE)

FIG. 27C

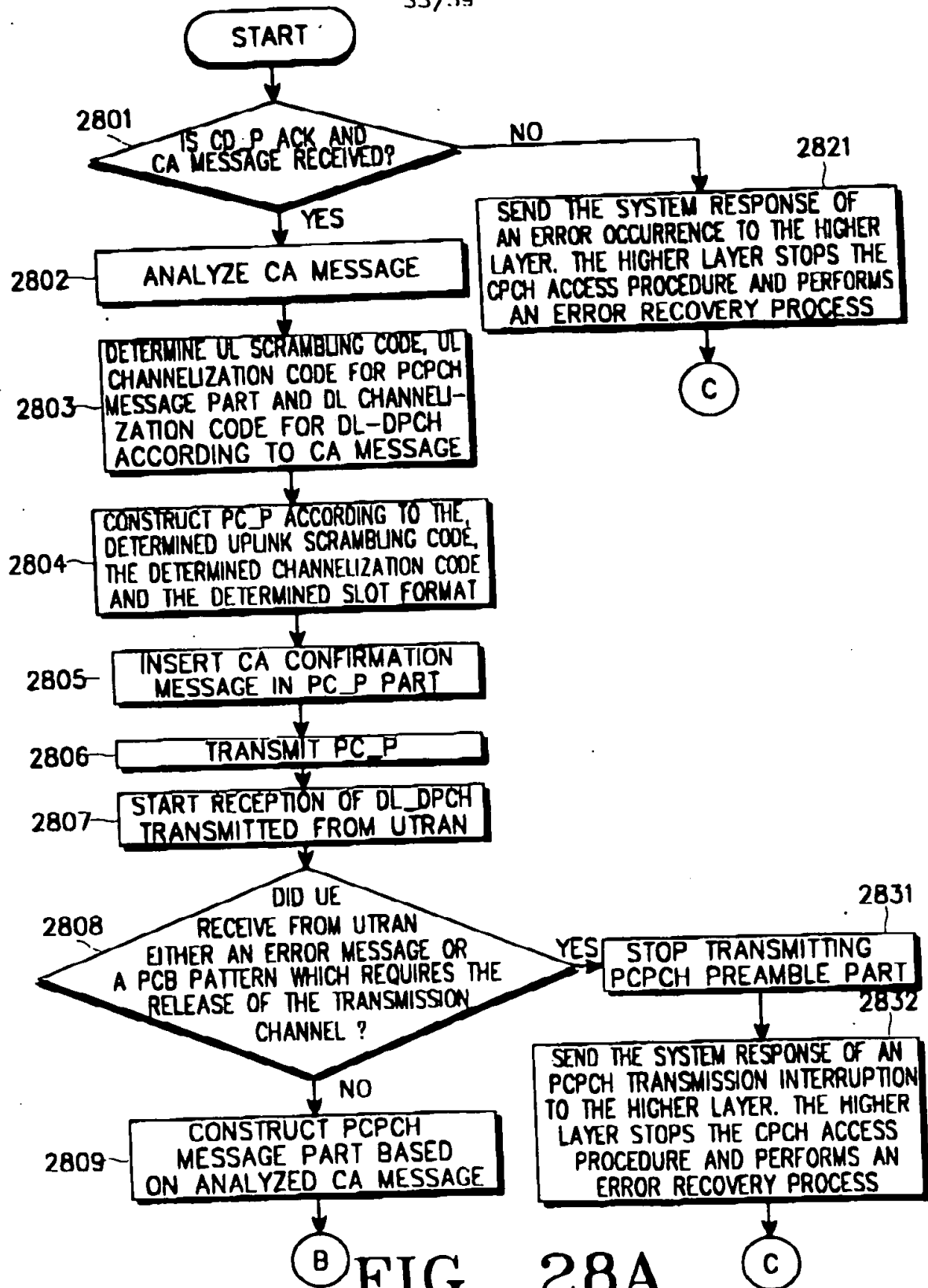


FIG. 28A

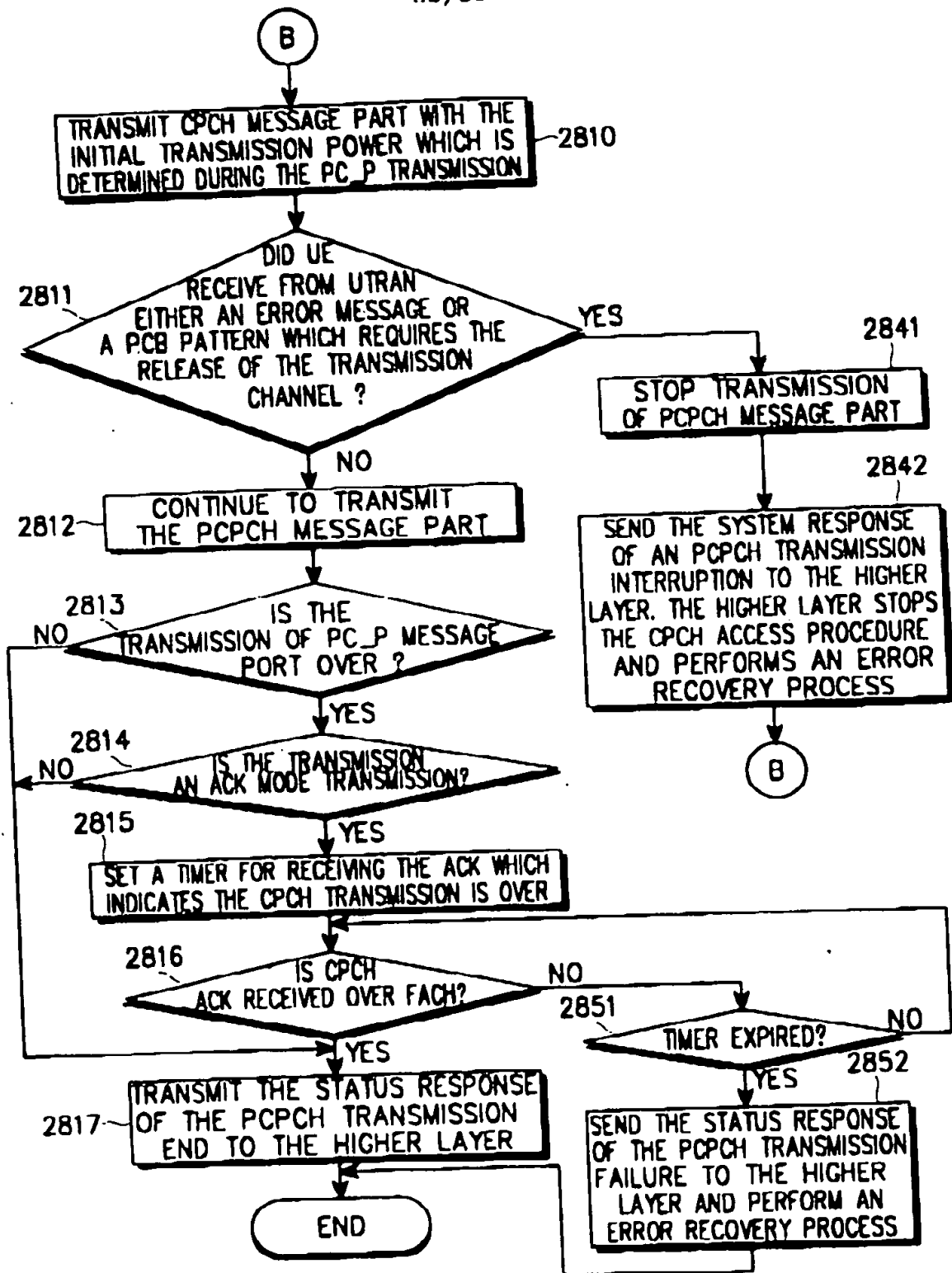


FIG. 28B

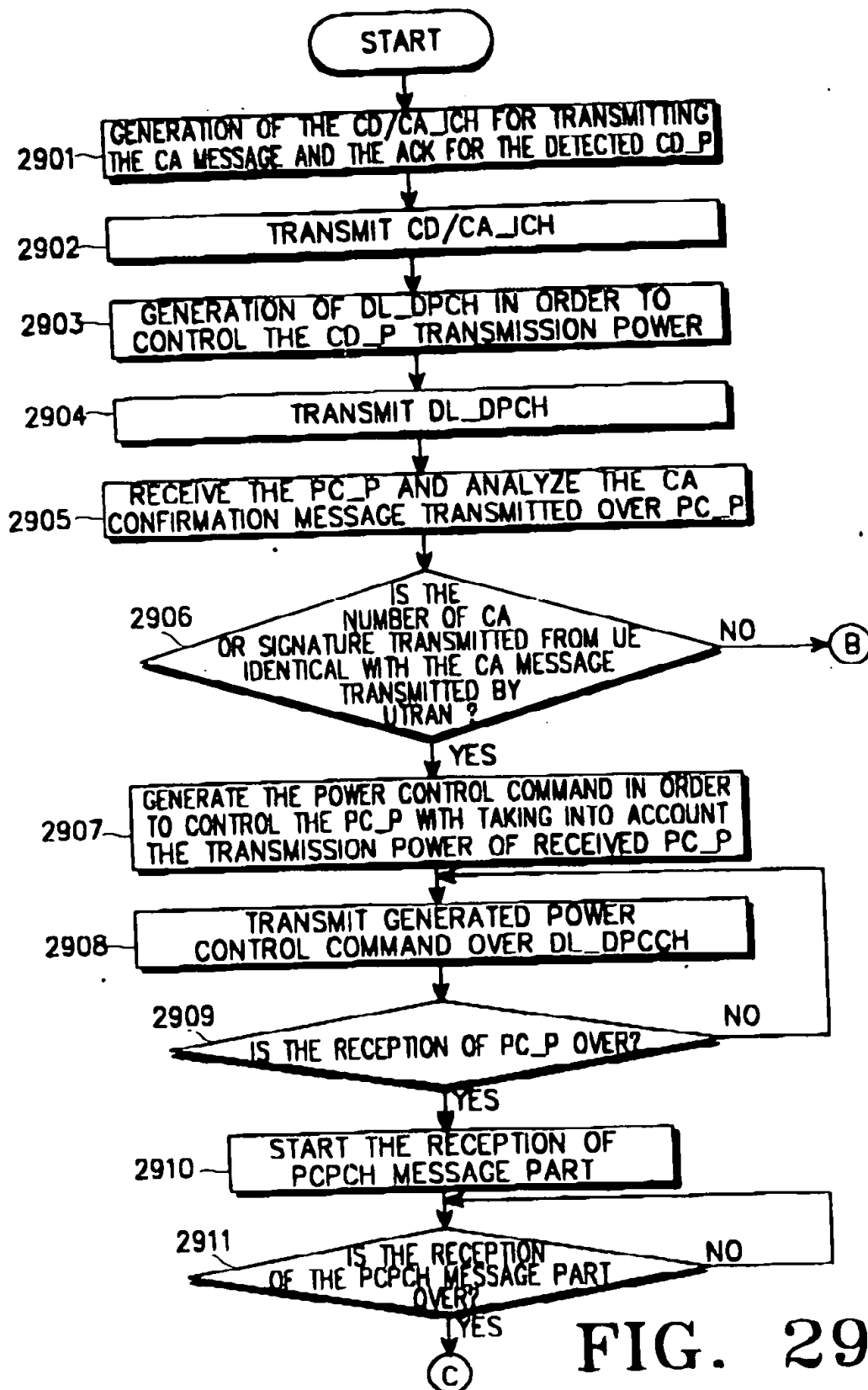


FIG. 29A

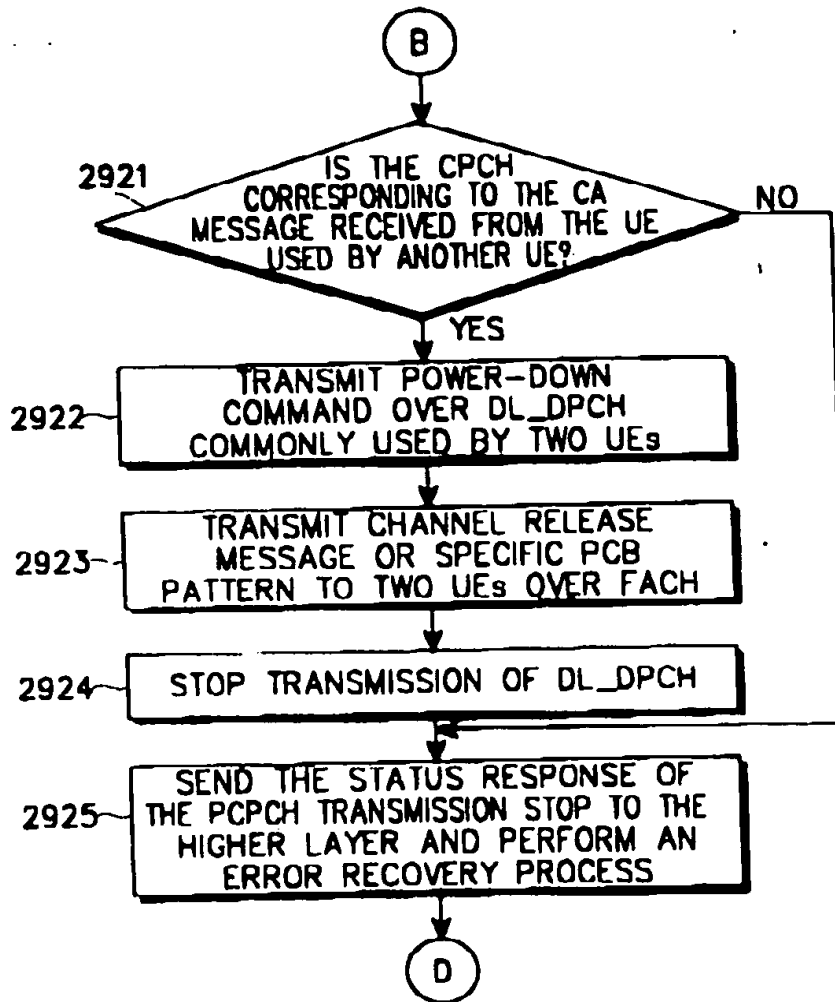


FIG. 29B

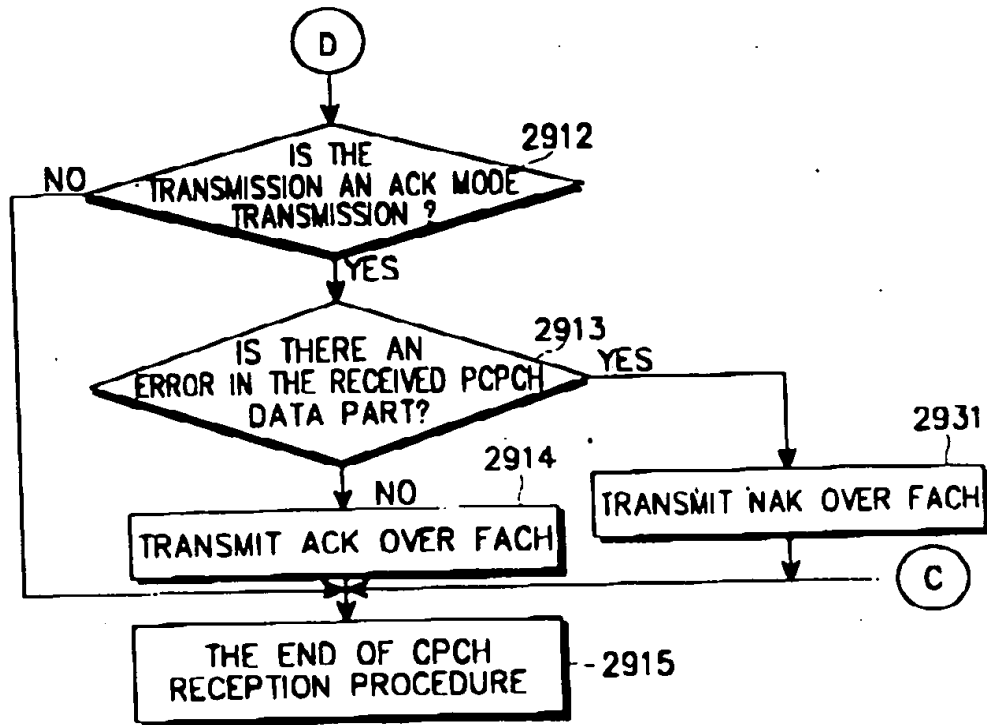


FIG. 29C